**Application No.: 10/828,263** 

## AMENDMENTS TO THE ABSTRACT

Please amend the abstract as follows. Please cancel the previous abstract, and substitute the new abstract presented below in clean text. The Applicants appreciate the suggestions by the Examiner for the wording of the new abstract.

## NEW ABSTRACT IN CLEAN TEXT:

An apparatus for testing a semiconductor device by mounting a plurality of chip intellectual properties (IPs) on a common semiconductor wiring substrate, including a silicon wiring substrate on which the chip IPs are mounted. A circuit for a boundary scan test is formed on the silicon wiring substrate by connecting flip-flops to wiring, which are arranged to test connections in the wiring. An IP on Super-Sub (IPOS) device or each chip IP may be arranged to facilitate a scan test, a built-in self-test (BIST), etc., on the internal circuit of the chip IP.